

# EXHIBIT 3

## 6 of 6



SN. 07/685, 878

350-116-267 02/27

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of )  
 DANIEL B. D'SOUZA ) Examiner: W. Burns  
 Serial No. 07/685,787 ) Art Unit: 267  
 Filed: April 15, 1991 ) San Francisco, CA 94111  
 For: ACTIVE PROBE CARD ) January 17, 1992

685 878

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, DC 20231 on January 17, 1992

Signed: Marcia D. Shea  
 Marcia D. Shea

PETITION UNDER 37 CFR 1.136  
 FOR EXTENSION OF TIME TO RESPOND

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Commissioner of Patents  
 and Trademarks  
 Washington, D. C. 20231

Sir:

Pursuant to 37 C.F.R. 1.136, applicant hereby requests a two-month extension of time in which to respond to the Office Action mailed September 10, 1991.

Enclosed is our Check No. 46420 in the amount of \$350.00. The Commissioner is hereby authorized to charge any other fees the Commissioner determines to be due or credit any overpayment, to Deposit Account 06-1300 (Order No. A-51856). A duplicate copy of this sheet is enclosed for such purpose.

Respectfully submitted,  
 FLEHR, HOHBACH, TEST,  
 ALBRITTON & HERBERT

James A. Sheridan  
 James A. Sheridan  
 Reg. No. 25,435  
 Tel. (415) 494-8700

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TWO  
~~ONE~~ MONTH EXTENSION GRANTED  
 By Direction  
 Primary Examiner

A-54681/JAS

O. Gordon 02-27-92  
 Clerk, Group 250 Date



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of )  
DANIEL B. D'SOUZA ) Examiner: W. Burns  
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A-54681/JAS

07/27



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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GROUP 250

AMENDMENT

Commissioner of Patents  
and Trademarks  
Washington, D. C. 20231

Sir:

In response to the Office Action dated September 10, 1991, please amend the application as follows:

IN THE ABSTRACT:

Please replace the Abstract with the following:

Abstract

An active probe card having integral test circuitry directly attached to the probe card. The probe card includes a circuit board wherein the test circuitry is mounted on the circuit board. In an alternate embodiment, the probe card also includes an on-board signal selection device. The test circuitry applies test signals through probe pins to integrated circuit input pads and samples the test signal responses at integrated circuit output pads. The orientation of the test circuitry attached to the each pin, i.e., input or output, is field programmable. The test circuitry may use boundary scan testing methodology. The active probe card's test circuitry may

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implement the test methodology of IEEE standard 1149.1 or analog test circuitry to determine the ac and dc parametric characteristics of the integrated circuit. The active probe card may include terminals to which Automatic Test Equipment (ATE) can be attached. *CH*

IN THE CLAIMS

On page 15, line 5, change "ports;" to "--ports; and--."

REMARKS

The Abstract has been amended to conform to the requirements of MPEP section 698.01(b).

Claims 1, 3 and 8 were rejected under 35 U.S.C. §102(e) as being anticipated by Wiscombe, Leedy, Cho or Petrich. Claim 4 was rejected as being anticipated by Cho; Claim 6 was rejected as being anticipated by Cho or Petrich; and Claim 7 was rejected as being anticipated by Petrich or Bove. Applicant respectfully traverses these rejections.

The invention is generally directed to a probe card for testing an integrated circuit wherein test circuitry is mounted on the probe card. In particular, the probe card is comprised of a circuit board and the test circuitry is mounted on the circuit board.

None of the references cited, teach or suggest a probe card having on-board test circuitry. Therefore, Claim 1 and Claims 2-8, which depend therefrom, are patentable over Wiscombe, Bove, Leedy, Cho and Petrich. U.S. Patent No. 5,020,219 to Leedy, for a Method of Making a Flexible Tester Surface for Testing Integrated Circuits, is directed to a flexible tester surface used to test a wafer during fabrication prior to metallization. It is not designed to test an integrated circuit as recited in claim 1. See Col. 2, lines 6-9. The tester surface is not a probe card as recited in Claim 1 nor is it a circuit board.

*2*

The tester surface has probe points on one side which, via fluid pressure, electrically contact the contacts on the wafer. Abstract; Col. 3, lines 26-27, 41-43, 63-67; Col. 4, lines 28-32. The tester surface is connected to a conventional tester signal processor separate from and external to the tester surface. See Col. 3, lines 50-54; FIG. 4A. Hence, the tester surface also does not include test circuitry mounted on the tester surface. Thus, the Leedy reference does not teach or suggest a probe card wherein the test circuitry is mounted on the card, as recited in Claim 1.

U.S. Patent No. 5,014,002 to Wiscombe et al. is directed to an ATE Jumper Programmable Interface Board for interconnecting automated test equipment and the pins of the integrated circuit device to be tested. See Col. 3, lines 21-25. The automated test equipment (ATE) is not integral to the interface board. Hence, the reference provides no teaching of the invention of Claim 1 wherein a probe card, comprised of a circuit board, has test circuitry mounted on the circuit board.

U.S. Patent No. 4,517,512 to Petrich et al. for an Integrated Circuit Test Apparatus Test Head also does not teach or suggest the invention of Claim 1. Petrich is directed to a test system within a test head module. The test head module is external to the probe card as well as the device under test. The reference states that the test head module may be as much as three to five feet away from the device under test. See Col. 5, lines 55-65. While Petrich states that the module could be miniaturized, there is no teaching or suggestion to place the test head module on the probe card itself. See Col. 7, lines 26-30.

U.S. Patent No. 4,038,599 to Bove et al. is directed to a High Density Wafer Contacting and Test System. The electronic test system (14, 15 and 12) is external to and separate from the probe assembly 20. The test system is

connected to the probe assembly via leads L1 and L3. There is no teaching or suggestion to mount test circuitry on the probe card, as recited in Claim 1. See Col. 7, lines 30-38; Col. 8, lines 14-30; FIG. 1. In fact, the 4,038,599 patent teaches that the tester is a "mini-computer or a more sizeable time-shared computer". See Col. 8, lines 26-28.

U.S. Patent No. 4,626,775 to Cho et al. for a RADIO FREQUENCY PROBING APPARATUS FOR SURFACE ACOUSTIC WAVE DEVICES includes a probe card. The probe card disclosed, however, does not have any test circuitry mounted thereon. See Col. 5, lines 35-65. The test computer and other test circuitry 103 are not mounted on the probe card. See Col. 2, lines 50-69; Col. 3, lines 1-21; FIGS. 1, 2 and 3.

Claim 1 recites that a probe card for testing integrated circuits is comprised of a circuit board and test circuitry mounted thereon. Since none of the references disclose a probe card having on-board test circuitry Claims 1, 3 and 8 are believed to be patentable over these references.

Claim 2 was rejected under 35 U.S.C. §103 as being obvious in light of Bove, Petrich, Leedy, Cho or Wiscombe. Claim 2 depends from claim 1. As previously discussed, since none of these references teach or suggest a probe card having test circuitry mounted thereon, Claim 1 is nonobvious and, therefore, Claim 2's recitation of test circuitry conforming with IEEE standard 1149.1 is nonobvious as well.

Claim 5 was rejected under 35 U.S.C. §103 as being obvious in light of Bove, Leedy or Wiscombe and further in view of U.S. Patent No. 4,465,972 to Sokolich. Applicant's invention is not met by the proposed combination, and therefore, Applicant respectfully traverses this rejection as well.

Claim 5 depends from Claim 1 and recites that the test circuitry "implements standardized boundary scan integrated circuit test techniques and methodology". Like Claim 2, since

none of the references suggest a probe card having on-board test circuitry, the specific test circuitry cited in Claim 5 would also be non-obvious.

Claims 9, 11 and 14-16 were rejected under 35 U.S.C. §102(e) as being anticipated by Petrich. Claims 11 and 14-16 depend from Claim 9. Claim 9, which is similar to Claim 1, is directed to an active probe card for testing an integrated circuit. The claimed probe card is comprised of a circuit board and test circuitry mounted on the circuit board. Claim 9 further recites that the test circuitry includes test signal selection means. Hence, the selection means are also on board the probe. Again, Petrich shows a test system 20 which is external to and separate from the probe 34. While Petrich teaches a device with a stack bus 102, the stack bus is part of the test head and is external to the probe card. See FIG. 1; Col. 7, lines 1-4; lines 15-30. Since the Petrich reference does not teach or suggest a probe card with on board test circuitry and an on board signal selection device, Claim 9 is patentable over Petrich.

Claim 9, and Claims 11 and 16 which depend therefrom, were also rejected under 35 U.S.C. §103 as being unpatentable over Bove, Leedy, Cho or Wiscombe and further in view of Hiwada et al. or Petrich. Again, Applicant's invention is not met by the proposed the proposed combination. None of the references alone, or in combination suggest including test circuitry, signal selection means, and conductive connection means on-board a probe card, as recited in Claim 9. Therefore, Claim 9 and Claims 11 and 16, which depend therefrom, are believed to be patentable over these references.

Claim 10 is also rejected under 35 U.S.C. §103 as being unpatentable over the combination of Petrich, Bove, Leedy, Cho or Wiscombe in view Hiwada. Again, since none of these references teach or suggest an on-board test circuitry, specific

on-board test circuitry which conforms to IEEE standard 1149.1 would also be nonobvious.

Claim 12 was rejected under 35 U.S.C. §103 as being obvious in light of Cho and Hiwada or Petrich; Claim 13 was rejected under 35 U.S.C. §103 as being obvious in light of Bove, Leedy or Wiscombe and Hiwada or Petrich and further in view of Sokolich; Claim 14 was rejected under 35 U.S.C. §103 as being unpatentable in view of the combination of Cho in view of Hiwada or Petrich; and Claim 15 was rejected under 35 U.S.C. §103 as being obvious in light of Bove and Hiwada or Petrich. Again, each of these claims depends from Claim 9. Since none of the references cited suggest a probe card having test circuitry mounted thereon, Claim 9, and Claims 12 -15 which depend therefrom, are nonobvious and therefore patentable over these references.

Furthermore, with respect to Claim 12, neither Hiwada or Petrich suggests including selection means on-board the probe card and, therefore, the invention of Claim 12 is non-obvious in light of these references.

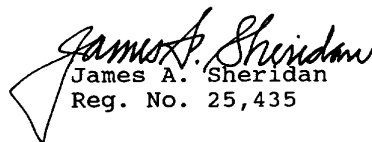
Similarly, since the idea of on-board test circuitry as recited in Claim 9 is nonobvious, Claim 13's specific recitation that the on-board test circuitry is implemented using standardized boundary scan integrated circuit test techniques and methodology, Claim 13 is nonobvious as well.

Claim 14's recitation that the on-board test circuitry includes analog circuits for measuring dc and ac parametric data is also not suggested by Cho, Hiwada or Petrich since none of these references even suggest including test circuitry on-board the probe card. Similarly, Claim 15's recitation that the on-board test circuitry further includes bi-directional cells is also nonobvious since Bove, Hiwada and Petrich do not even suggest including test circuitry on-board on the probe card.

In conclusion, since none of the references cited by the Examiner either alone, or in combination, teach or suggest a probe card which includes test circuitry mounted on the probe card itself, Claims 1 and 9, and the claims which depend therefrom, are believed patentable over these references. In light of the foregoing, early allowance of this application is respectfully requested. The Examiner is encouraged to contact the undersigned to discuss this amendment further.

Respectfully submitted,

FLEHR, HOHBACH, TEST,  
ALBRITTON & HERBERT

  
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Reg. No. 25,435

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**UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office**

 Address : COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
07/685,878	04/15/91	D'SOUZA	A-54691/JAS

 EXAMINER  
BURNS, W

 FLEHR, HOHBACH, TEST  
ALBRITTON & HERBERT  
STE. 3400, FOUR EMBARCADERO CENTER  
SAN FRANCISCO, CA 94111

ART UNIT	PAPER NUMBER
2607	7

DATE MAILED: 05/04/92

 This is a communication from the examiner in charge of your application.  
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined     
 ☒ Responsive to communication filed on 1/21/92     
 ☒ This action is made final.

 A shortened statutory period for response to this action is set to expire 3 month(s), — days from the date of this letter.  
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

**Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:**

- |   |  |
|---|--|
| 1. <input type="checkbox"/> Notice of References Cited by Examiner, PTO-892.        | 2. <input type="checkbox"/> Notice re Patent Drawing, PTO-948.                   |
| 3. <input type="checkbox"/> Notice of Art Cited by Applicant, PTO-1449.             | 4. <input type="checkbox"/> Notice of Informal Patent Application, Form PTO-152. |
| 5. <input type="checkbox"/> Information on How to Effect Drawing Changes, PTO-1474. | 6. <input type="checkbox"/> _____  |

**Part II SUMMARY OF ACTION**

1. ☒ Claims 1-16 are pending in the application.  
Of the above, claims \_\_\_\_\_ are withdrawn from consideration.
2. ☐ Claims \_\_\_\_\_ have been cancelled.
3. ☐ Claims \_\_\_\_\_ are allowed.
4. ☒ Claims 1-16 are rejected.
5. ☐ Claims \_\_\_\_\_ are objected to.
6. ☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on \_\_\_\_\_. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on \_\_\_\_\_ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed on \_\_\_\_\_, has been ☐ approved. ☐ disapproved (see explanation).
12. ☐ Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received  
☐ been filed in parent application, serial no. \_\_\_\_\_; filed on \_\_\_\_\_.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

Serial No. 685,878

-2-

Art Unit 2607

1. Applicant's arguments filed 1/21/92, stating that Wiscombe, Leedy, Cho, Bove, and Petrich do not show test circuitry upon a probe card; that Leedy does not show IC testing; and that Petrich does not show selection circuitry upon a probe card have been fully considered but they are not deemed to be persuasive.

Wiscombe (see card 18, and conductors thereon); Cho (see card 325 and conductors and components thereon); Leedy (see card 10, with conductors thereon); Petrich (see card 88, with conductors and components thereon); and Bove (see card 20, with conductors thereon) each show probe-mounting cards which also mount conductor lines and/or electrical components which are used to test a circuit. The lines and components thus are "test circuitry" meeting this limitation in the claims. While other circuitry may be mounted away from the card, there is no recited limitation in the claims as to all circuitry used for test purposes as being on the card, thus still enabling the applied references to meet the claim limitations.

As to Leedy's teachings; Leedy teaches (see col. 2, lines 6, 7) of testing incomplete IC's, in the process of manufacture. The transistors (see col. 2, lines 63-65) are complete on each IC, with only the metal interconnections to be completed. These incomplete IC's thus are deemed to be "IC"'s for purposes of testing, as the semiconductor components have already been completed. Thus, Leedy is deemed to show testing of IC's.

Serial No. 685,878

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Art Unit 2607

As to Petrich's teachings; a card member (88) houses probes, and a multitude of electrical test circuit components (84, 86, 102, 105, et al). Switching circuitry (102, see fig. 2, and col. 12, lines 29-31) is mounted upon the card.

Applicant cites col. 7, lines 1-4 and 15-30 as showing that component 102 is not upon the card, yet there is no mention of 102 in those cited lines of the Petrich disclosure. Col. 12, lines 29-31, and fig. 2 of Petrich, however, specifically show 102 as upon the card; and thus Petrich does indeed show on-card switching circuitry.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1, 3, and 8 are rejected under 35 U.S.C. § 102(b) as being anticipated by Bove et al, Wiscombe, Petrich, Leedy, or Cho.

Wiscombe et al, Bove et al, Leedy, Cho, and Petrich each show a circuit board with test circuitry thereupon, with test

Serial No. 685,878

-4-

Art Unit 2607

signal ports, and connectors connecting to connectors of tested circuitry. The connecting means comprises conductive traces, pads, and probe pins.

4. Claim 4 is rejected under 35 U.S.C. § 102(e) as being anticipated by Cho.

Cho applies as above, and in addition shows a central aperture, with probe pins extending into it.

5. Claim 6 is rejected under 35 U.S.C. § 102(e) as being anticipated by Cho or Petrich.

Cho and Petrich each apply as for claims 1, 3, and 8, and in addition show ac/dc parametric testing with analog circuitry.

6. Claim 7 is rejected under 35 U.S.C. § 102(e) and (b) as being anticipated by Petrich or Bove et al.

Bove et al applies as for claims 1, 3, and 8, and in addition shows test circuitry (figs. 2, 3) comprising bi-directional, user-oriented cells. Petrich applies as for claims 1, 3, and 8, and in addition (see fig. 7) shows bi-directional "pin electronics cards" cells being configured by a user for testing.

7. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary

Serial No. 685,878

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Art Unit 2607

skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

8. Claim 2 is rejected under 35 U.S.C. § 103 as being unpatentable over Bove, or Petrich, or Leedy, or Cho, or Wiscombe.

Bove, Petrich, Leedy, Cho, and Wiscombe apply as for claims 1, 3, and 8. In addition, it would be a matter of conventional design choice to configure the circuitry to IEEE std. 1149.1 given that is an official, conventional standard, able to make with many types of tested circuits.

9. Claim 5 is rejected under 35 U.S.C. § 103 as being unpatentable over Bove, Leedy, or Wiscombe as applied to claims 1, 3, and 8 above, and further in view of Sokolich.

Sokolich shows a probe card (component 16) comprising scan-testing shift registers.

It would have been obvious to one ordinarily-skilled in the art to modify the apparatus of Bove, Leedy, or Wiscombe as taught by Sokolich, to provide shift registers for the test circuitry, in order to efficiently parallel test a multitude of IC circuits quickly; and to further modify to (in particular to boundary

Serial No. 685,878

-6-

Art Unit 2607

scan-testing) using the shift registers, in order to accurately test complex IC circuitry.

10. Claims 9, 11, and 14-16 are rejected under 35 U.S.C. § 102(e) as being anticipated by Petrich.

Petrich applies as for claims 1, 3, and 8; and in addition shows selection means (component 102 of fig. 7) which can select internal (from components 88, 84, 86 et al) or external (from component 60) test signals.

11. Claims 9, 11, and 16 are rejected under 35 U.S.C. § 103 as being unpatentable over Bove or Leedy or Cho or Wiscombe as applied to claims 1, 3, and 8 above, and further in view of Petrich.

Petrich shows a test head apparatus with test circuitry selecting either internal or external test signals.

It would have been obvious to one ordinarily-skilled in the art to modify the test apparatus of Bove or Leedy or Cho or Wiscombe as taught by Petrich, to enable a wider array of test signals to be generated (permitting more comprehensive testing) by providing internal/external test selection means.

12. Claim 10 is rejected under 35 U.S.C. § 103 as being unpatentable over Petrich or Bove or Leedy or Cho or Wiscombe; in view of Petrich.

Petrich, Bove, Leedy, Cho, Wiscombe, and Hiwada each apply as discussed above. In addition, it would further be a matter of

Serial No. 685,878

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Art Unit 2607

conventional design choice to have the test head follow IEEE std. 1149.1, as discussed for claim 2.

13. Claim 12 is rejected under 35 U.S.C. § 103 as being unpatentable over Cho as applied to claims 4, 9, 11, and 16 above, and further in view of Petrich.

Cho and Petrich apply as for claims 9, 11, and 16. It would have been obvious to one ordinarily-skilled in the art to modify the apparatus of Cho as taught by Petrich, as discussed for claims 9, 11, and 16.

14. Claim 13 is rejected under 35 U.S.C. § 103 as being unpatentable over Bove, Leedy, or Wiscombe in view of Petrich as applied to claims 9, 11, and 16 above, and further in view of Sokolich.

Sokolich applies as for claim 5. It would have been obvious to one ordinarily-skilled in the art to modify the apparatus of Bove, Leedy, or Wiscombe as taught by Petrich; and to further modify as taught by Sokolich as per claim 5.

15. Claim 14 is rejected under 35 U.S.C. § 103 as being unpatentable over Cho in view of Petrich.

Cho and Petrich, apply as for claims 9, 11, and 16, and in addition, Cho shows ac/dc parametric testing.

16. Claim 15 is rejected under 35 U.S.C. § 103 as being unpatentable over Bove in view of Petrich.

Bove and Petrich apparently as for claims 9, 11, and 16; and

Serial No. 685,878

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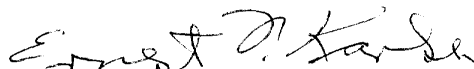
Art Unit 2607

in addition Bove shows bi-directional cells which are user-oriented.

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

W.B.5/1/92  
W. Burns:tlr  
April 30, 1992

  
ERNEST F. KARLSEN  
PRIMARY EXAMINER  
GROUP 267



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of )

DANIEL B. D'SOUZA )

Serial No. 07/685,878 )

Filed: April 15, 1991 )

For: ACTIVE PROBE CARD )

Examiner: W. Burns )

Art Unit: 2607 )

San Francisco, CA )

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, DC 20231 on July 24, 1992.

Signed: Barbra Sheridan

Barbra Sheridan

AMENDMENT

Commissioner of Patents  
and Trademarks  
Washington, D. C. 20231

Sir:

In response to the Office Action dated May 4, 1992, please amend the application as follows:

REMARKS

The Applicant notes that the Examiner has not found the arguments included in the Amendment dated January 21, 1992 to be persuasive. The Applicant has included herein more detailed arguments distinguishing the present invention from the cited prior art.

Claims 1, 3 and 8 were rejected under 35 U.S.C. §102(b) as being anticipated by Wiscombe, Leedy, Cho or Petrich. Claim 4 was rejected under 35 U.S.C. §102(e) as being anticipated by Cho. Claim 6 was rejected under 35 U.S.C. §102(e) as being

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anticipated by Cho or Petrich. Claim 7 was rejected under 35 U.S.C. §102(e) and (b) as being anticipated by Petrich or Bove.

Claim 2 was rejected under 35 U.S.C. §103 as being unpatentable over Bove, Petrich, or Leedy, or Cho, or Wiscombe. Claim 5 was rejected under 35 U.S.C. §103 as being unpatentable over Bove, Leedy, or Wiscombe in view of Sokolich. Claims 9, 11, and 14-16 were rejected under 35 U.S.C. §102(e) as being anticipated by Petrich. Claims 9, 11, and 16 were rejected under 35 U.S.C. §103 as being unpatentable over Bove or Leedy or Cho or Wiscombe in view of Petrich. Claim 10 was rejected under 35 U.S.C. §103 as being unpatentable over Bove or Leedy or Cho or Wiscombe in view of Petrich. Claims 12 and 15 were rejected under 35 U.S.C. §103 as being unpatentable over Cho in view of Petrich. Claim 13 was rejected under 35 U.S.C. §103 as being unpatentable over Bove, Leedy, or Wiscombe in view of Petrich and Sokolich. Claim 14 was rejected under 35 U.S.C. §103 as being unpatentable over Cho in view of Petrich. The Applicant respectfully traverses these rejections

The invention is generally directed to a probe card for testing an integrated circuit wherein test circuitry and the integrated circuit to be tested are mounted on the probe card. In particular, the probe card is comprised of a circuit board to which the test circuitry and the integrated circuit to be tested are directly mounted. These limitations are clearly described in Claims 1 and 9, the only independent claims in the application. Line 4 of Claims 1 and 9 states: "test circuitry mounted on said circuit board .....". Lines 6-9 of Claims 1 and 9 state: "means for conductively connecting said plurality of test signal ports to an array of connectors of the integrated circuit under test." These portions of Claims 1 and 9 clearly limit the present invention to a probe card on which the test circuitry and the integrated circuit under test are directly connected.

None of the references cited, teach or suggest a probe card having on-board test circuitry and means to attach the circuit to be tested directly to the probe card. Therefore, Claim 1 and Claim 9, and Claims 2-8 and 10-16, which depend therefrom, are patentable over Wiscombe, Bove, Leedy, Cho, Petrich, and Sokolich.

The Applicant notes the Examiner's argument that U.S. Patent No. 5,020,219 (Leedy) is deemed to show testing of IC's. However, the Applicant would like to stress that the key feature that distinguishes the present invention from the Leedy patent is not the testing of IC's, but rather the mounting of the test circuitry onto the probe card. The test surface of Leedy does not contain test circuitry. Rather, the test circuitry in Leedy is housed in an externally mounted tester signal processor as shown in Figure 4a and described in Column 3, lines 50-59. In the present invention, the test circuitry is attached directly to the probe card. This allows for the direct connection between the device under test and the test circuitry, thereby eliminating costly time delay and impedance mismatch circuitry (See page 3, lines 25-30). Thus, the Leedy reference does not teach or suggest a probe card wherein the test circuitry is mounted directly on the card, as recited in Claim 1 and Claim 9.

U.S. Patent No. 4,517,512 (Petrich et al.) for an Integrated Circuit Test Apparatus Test Head also does not teach or suggest the present invention. As shown in Figure 2, Petrich discloses a test system comprising a test head module 28 comprising mother board 82, functional circuit boards 84, 86, and 88, and pin electronics cards 105. The mother board and circuit boards perform the desired test functions of the test system (Column 25, lines 17-23). However, the circuit boards of the test head module 28 are external to the device under test 50. The reference states that the test head module

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49-52

NP  
may be as much as three to five feet away from the device under test. See Col. 5, lines 55-65. As described in column 24, lines 18-65 and shown in Figure 2, the test circuitry of the mother board 82 and circuit boards 84, 86, 88, are connected to the pin electronics card 105. Terminals 105b of the pin electronics card 105 are connected to the contact pads of the character board 49. The conductor paths of the character board 49 are connected to the respective pins of the device under test 50. Therefore, the Petrich reference does not teach or suggest a probe card wherein the test circuitry is mounted directly on the card, as recited in Claim 1 and Claim 9.

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U.S. Patent No. 5,014,002 to Wiscombe et al. is directed to an ATE Jumper Programmable Interface Board for interconnecting automated test equipment and the pins of the integrated circuit device to be tested. See Figure 2 and Col. 3, lines 21-25. The interface board 18 does not implement a testing methodology such as the IEEE standard 1149.1 as does the interface board of the present invention. Rather, the interface board of Wiscombe simplifies the process of setting up the interconnections between the device to be tested 14 and the test head module 12. See Figure 2 and Column 5, lines 7-17. Hence, the reference provides no teaching of the invention of Claim 1 wherein a probe card, comprised of a circuit board, has test circuitry mounted on the circuit board.

U.S. Patent No. 4,038,599 (Bove et al.) for an Integrated Circuit Test Apparatus Test Head also does not teach or suggest the present invention. The Examiner states in the Office Action dated May 4, 1992 that the conductors 19 on the probe card 20 are "test circuitry" as described in the claims of the present invention. The Applicant respectfully submits that the simple conductors of Bove, such as those shown as 19 (Figure 1) on the probe card 20, can not possibly be test circuitry as defined in the claims of the present invention. Although the

*app p 17, lines 24-25 - "illustrative, not limiting" for "analog circuitry" for "ac, dc parametric characteristics"*  
 claim mentions only "test circuitry", the Applicant respectfully submits that meaning of the terms in the claims should be derived from the description in the specification. Paragraph 608.01(o) of the M.P.E.P. states: "The meaning of every term used in any of the claims should be apparent from the descriptive portion of the specification with clear disclosure as to its import." §1.75(d)(1) of 37 CFR states that "... the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description." As described in the summary of the specification on page 4, lines 17-30, and in more detail on line 13, page 8, through line 24, page 10, the test circuitry of the present invention implements the test procedure used to evaluate the integrated circuit. This test circuitry 203 (Figure 2), which is mounted directly to the probe card 200, can be used to implement a boundary-scan testing methodology such as the IEEE standard 1149.1. The simple conductors 19 of Bove can not possibly implement such a test procedure and therefore Bove does not teach or suggest a probe card wherein the test circuitry is mounted directly on the card. In fact, Bove utilizes external test circuitry 14 and 15 to accomplish the function of the test circuitry 203 on the probe card of the present invention. The test circuitry 14 and 15 of Bove supplies the test patterns to the device to be tested. (Column 8, lines 59-64) This test circuitry is external to and separate from the probe assembly 20. The test system is connected to the probe assembly via leads L1 and L3. See Col. 7, lines 30-38; Col. 8, lines 14-30; and Figure. 1. Bove also teaches that the tester is a "mini-computer or a more sizeable time-shared computer". See Col. 8, lines 26-28. Therefore, the conductive pins of Bove can not possibly act as the test circuitry of the present invention as claimed. Thus,

the Bove reference does not teach or suggest a probe card wherein the test circuitry is mounted directly on the card.

U.S. Patent No. 4,626,775 to Cho et al. for a RADIO FREQUENCY PROBING APPARATUS FOR SURFACE ACOUSTIC WAVE DEVICES includes a probe card. The probe card disclosed, however, does not have any test circuitry mounted thereon. See Col. 5, lines 35-66. The test computer and other test circuitry 103 are not mounted on the probe card. See Col. 2, lines 50 - Col. 3, lines 21; FIGS. 1, 2 and 3.

U.S. Patent No. 4,465,972 (Sokolich) discloses a printed circuit board testing apparatus. The test apparatus comprises an insulating plate 10 for connecting the printed circuit board under test to a plurality of circuit boards mounted perpendicular to the insulating plate. Mounted on the perpendicular circuit boards are integrated circuits which are used to make short and continuity tests of the printed circuit board under test. See Figures 3 and 4, and Column 4, lines 29-46. However, Sokolich does not teach a probe card which is directly attached to the device under test and the test circuitry. The device under test is not directly connected to the integrated test circuits 19. Instead, the device under test is connected to the test circuitry via the insulating plate 10 and the plurality of circuit boards 16. (See Figure 3). Thus, the Sokolich reference does not teach or suggest a probe card wherein the test circuitry is mounted directly on the card.

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Claim

Claims 1, 3, 4, 6, 7, 8, 9, 11, 14-16 were rejected under 35 U.S.C. §102(b) and/or §102(e). The Applicant respectfully submits that the standard for anticipation under 35 U.S.C. § 102 is one of strict identity. 1D. Chisum, Patents, Section 3.02 at 3-6 (1991). Thus, an anticipation rejection requires showing that each limitation of a claim must be found in a

single reference. In re Donohue, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621, (Fed. Cir. 1985). If a reference simply fails to include just one of the claimed limitations, this is enough to negate anticipation by that reference. Atlas Powder Co. v. E.I. du Pont De Nemours & Co., 750 F.2d. 1569, 1574, 224 U.S.P.Q. 409, 411 (Fed. Cir. 1984). In applying this standard to the present case, it is clear that none of the cited references anticipate the rejected independent Claims 1 and 9 in view of the above argument. None of the references disclose a probe card having on-board test circuitry and means to attach the circuit to be tested directly to the probe card as described in independent Claim 1. Also, as described in the only other independent Claim 9, none of the references disclose a probe card having on-board test circuitry including test signal selection means, and means to attach the circuit to be tested directly to the probe card. Therefore, the independent Claims 1 and 9 are not anticipated by the cited references. Since Claims 3, 4, 6, 7, 8, 11, 14-16 depend on Claims 1 and 9, these claims are also not anticipated by the cited references. Therefore, it is respectfully submitted that the Examiner's rejections under 35 U.S.C. § 102 have been overcome.

Claims 2, 5, and 9-16 were rejected under 35 U.S.C. §103. The Applicant respectfully reminds the Examiner that obviousness can not be established "absent some teaching or suggestion supporting the combination". ACS Hospital Systems, Inc. v. Montefiore Hospital, 221 USPQ 929, 933 (Fed. Cir. 1984). This standard has been repeatedly established in the Federal Circuit. The court in In re Newell stated that "[i]t is well established that in deciding that a novel combination would have been obvious, there must be some supporting teaching in the prior art." 13 USPQ 1248, 1250 (Fed. Cir. 1989). The Court continued, "[t]he critical inquiry is whether there is something in the prior art as a whole to suggest the

desirability, and thus the obviousness of making the combination." (Emphasis in original). (Citations omitted). Id. at 1250. Claim 1 describes a probe card for testing integrated circuits having test circuitry mounted directly on the probe card and means to mount the device under test directly to the card. As previously discussed, none of the cited references teach or suggest a probe card having test circuitry mounted thereon and means to mount the device under test directly to the card. Therefore, Claim 1 is nonobvious and, Claim 2's recitation of test circuitry conforming with IEEE standard 1149.1 is nonobvious as well.

Claim 5 was rejected under 35 U.S.C. §103 as being obvious in light of Bove, Leedy or Wiscombe and further in view of U.S. Patent No. 4,465,972 to Sokolich. As argued above for Claim 2, since none of the references teach or suggest a probe card having on-board test circuitry and means to mount the device under test directly to the card, the specific test circuitry cited in Claim 5 would also be non-obvious.

Claim 9, and Claims 11 and 16 which depend therefrom, were also rejected under 35 U.S.C. §103 as being unpatentable over Bove, Leedy, Cho or Wiscombe and further in view of Petrich. Again, Applicant's invention is not met by the proposed combination. None of the references alone, or in combination suggest or teach test circuitry, signal selection means, conductive connection means mounted directly to a probe card, and means to mount the device under test directly to the card as recited in Claim 9. Therefore, Claim 9 and Claims 11 and 16, which depend therefrom, are believed to be patentable over these references.

Claim 10 is also rejected under 35 U.S.C. §103 as being unpatentable over the combination of Petrich, Bove, Leedy, Cho or Wiscombe in view of Petrich. Again, since none of these references teach or suggest an on-board test circuitry,

specific on-board test circuitry which conforms to IEEE standard 1149.1 would also be nonobvious.

Claim 12 was rejected under 35 U.S.C. §103 as being obvious in light of Cho in view of Petrich; Claim 13 was rejected under 35 U.S.C. §103 as being obvious in light of Bove, Leedy or Wiscombe in view of Petrich and further in view of Sokolich; Claim 14 was rejected under 35 U.S.C. §103 as being unpatentable in view of the combination of Cho in view of Petrich; and Claim 15 was rejected under 35 U.S.C. §103 as being obvious in light of Bove in view of Petrich. Again, each of these claims depends from Claim 9. Since none of the references cited suggest a probe card having test circuitry mounted thereon and means to mount the device under test directly to the card as described in Claim 9, Claims 12-15, which depend therefrom, are nonobvious and therefore patentable over these references.

Similarly, since the idea of on-board test circuitry as recited in Claim 9 is nonobvious, Claim 13's specific recitation that the on-board test circuitry is implemented using standardized boundary scan integrated circuit test techniques and methodology is nonobvious as well.

Claim 14's recitation that the on-board test circuitry includes analog circuits for measuring dc and ac parametric data is also not suggested by Cho or Petrich since none of these references even suggest including test circuitry on-board the probe card. Similarly, Claim 15's recitation that the on-board test circuitry further includes bi-directional cells is also nonobvious since Bove and Petrich do not teach or suggest including test circuitry on-board on the probe card.

In conclusion, since none of the references cited by the Examiner either alone, or in combination, teach or suggest a probe card having test circuitry mounted directly to the probe card itself and means to attach the device to be tested

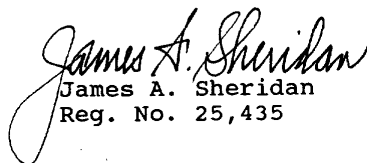
directly to the probe card, the Applicant respectfully submits that the Examiner's objections under 35 U.S.C. §102 and 35 U.S.C. §103 have been overcome. Claims 1 and 9, and the claims which depend therefrom, are believed patentable over the cited references.

directly to the probe card, the Applicant respectfully submits that the Examiner's objections under 35 U.S.C. §102 and 35 U.S.C. §103 have been overcome. Claims 1 and 9, and the claims which depend therefrom, are believed patentable over the cited references.

In light of the foregoing, this application is believed to be in condition for allowance and early allowance of this application is respectfully requested. The Examiner is encouraged to contact the undersigned to discuss this amendment further.

Respectfully submitted,

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Patent and Trademark Office  
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SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY CODE NO.
07/685,878	04/15/91	D'SOUZA	D A-54691/JAS

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2607	9
DATE MAILED	

08/04/92

Below is a communication from the EXAMINER in charge of this application

# COMMISSIONER OF PATENTS AND TRADEMARKS

## ADVISORY ACTION

### ☒ THE PERIOD FOR RESPONSE:

- a) ☐ is extended to run \_\_\_\_\_ or continues to run \_\_\_\_\_ from the date of the final rejection
- b) ☒ expires three months from the date of the final rejection or as of the mailing date of this Advisory Action, whichever is later. In no event however, will the statutory period for the response expire later than six months from the date of the final rejection.

Any extension of time must be obtained by filing a petition under 37 CFR 1.136(a), the proposed response and the appropriate fee. The date on which the response, the petition, and the fee have been filed is the date of the response and also the date for the purposes of determining the period of extension and the corresponding amount of the fee. Any extension fee pursuant to 37 CFR 1.17 will be calculated from the date of the originally set shortened statutory period for response or as set forth in b) above.

☐ Appellant's Brief is due in accordance with 37 CFR 1.193(a).

☒ Applicant's response to the final rejection, filed 5/4/92 has been considered with the following effect, but it is not deemed to place the application in condition for allowance:

1. ☐ The proposed amendments to the claim and /or specification will not be entered and the final rejection stands because:
- ☐ There is no convincing showing under 37 CFR 1.116(b) why the proposed amendment is necessary and was not earlier presented.
  - ☐ They raise new issues that would require further consideration and/or search. (See Note).
  - ☐ They raise the issue of new matter. (See Note).
  - ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal.
  - ☐ They present additional claims without cancelling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

2. ☐ Newly proposed or amended claims \_\_\_\_\_ would be allowed if submitted in a separately filed amendment cancelling the non-allowable claims.

3. ☒ Upon the filing an appeal, the proposed amendment ☐ will be entered ☒ will not be entered and the status of the claims will be as follows:

Claims allowed: \_\_\_\_\_

Claims objected to: \_\_\_\_\_

Claims rejected: 1-16

However;

☐ Applicant's response has overcome the following rejection(s): \_\_\_\_\_

4. ☒ The affidavit, exhibit or request for reconsideration has been considered but does not overcome the rejection because claim 1 and 9 do not specify what sort of "test equipment" has to be mounted on the probe cart; not the degree of proximity between the cart and IC
5. ☐ The affidavit or exhibit will not be considered because applicant has not shown good and sufficient reasons why it was not earlier presented.

☐ The proposed drawing correction ☐ has ☐ has not been approved by the examiner.

☐ Other

*Ernest F. Karlson*  
ERNEST F. KARLSEN  
PRIMARY EXAMINER  
GROUP 267


**UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office**

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SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/685,878	04/13/91	D'SOUZA	A-54691/JAS

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EXAMINER	
BURNS, W	
ART UNIT	PAPER NUMBER
	10

DATE MAILED:

11/09/92

**NOTICE OF ABANDONMENT**

This application is abandoned in view of:

- ☐ Applicant's failure to respond to the Office letter, mailed \_\_\_\_\_.
- ☐ Applicant's letter of express abandonment which is in compliance with 37 C.F.R. 1.138.
- ☐ Applicant's failure to timely file the response received \_\_\_\_\_ within the period set in the Office letter.
- ☐ Applicant's failure to pay the required issue fee within the statutory period of 3 months from the mailing date of \_\_\_\_\_ of the Notice of Allowance.

☐ The issue fee was received on \_\_\_\_\_.

☐ The issue fee has not been received in Allowed Files Branch as of \_\_\_\_\_.

In accordance with 35 U.S.C. 151, and under the provisions of 37 C.F.R. 1.316(b), applicant(s) may petition the Commissioner to accept the delayed payment of the issue fee if the delay in payment was unavoidable. The petition must be accompanied by the issue fee, unless it has been previously submitted, in the amount specified by 37 C.F.R. 1.17 (i), and a verified showing as to the causes of the delay.

If applicant(s) never received the Notice of Allowance, a petition for a new Notice of Allowance and withdrawal of the holding of abandonment may be appropriate in view of *Delgar Inc. v. Schuyler*, 172 U.S.P.Q. 513.

- ☐ Applicant's failure to timely correct the drawings and/or submit new or substitute formal drawings by \_\_\_\_\_ as required in the last Office action.

☐ The corrected and/or substitute drawings were received on \_\_\_\_\_.

- ☒ The reason(s) below.

*Applicant's continuing application filed under 37 CFR 1.62*

*Kenneth A. Wieder*  
KENNETH A. WIEDER  
SUPERVISORY PATENT EXAMINER  
ART UNIT 267A